CLAIMS

What is claimed is:

1. A semiconductor die comprising a plurality of dummy fillings positioned and sized to minimize defects during chemical mechanical polishing, at least one of the dummy fillings being coupled to an underlying test structure.

2. A semiconductor die as recited in claim 1, the semiconductor die further comprising:

a plurality of conductive layers; and

a substrate,

wherein the underlying test structure comprises a first layer portion formed from a first one of the plurality of conductive layer and a via coupling the first layer portion to the at least one dummy filling.

3. A semiconductor die as recited in claim 2, the underlying test structure further comprising a via coupling the first layer portion to the substrate.

4. A semiconductor die as recited in claim 3, wherein the underlying test structure comprises a plurality of layer portions and vias to form a multilevel test structure.

5. A semiconductor die as recited in claim 3, wherein the via is a redundant via.

6. A semiconductor die as recited in claim 3, wherein at least one of the vias coupled between the plurality of layers and between the underlying test structure and the first layer portion is a redundant via.

7. A method of fabricating a semiconductor die, comprising:

forming a plurality of conductive layers;

forming a test structure from at least one of the plurality of conductive layers; and

adding dummy fillings within a top conductive layer of the plurality of conductive layers so as to minimize defects from CMP, wherein at least on of the dummy filling is formed over the test structure.

8. A test pattern comprising a row of substantially parallel metal lines on a semiconductor die, the test pattern comprising:

a. a first plurality of substantially parallel metal lines, wherein (1) the metal lines are spaced apart by spaces of width W_1, (2) each of the metal lines has a width of W_1, and (3) the metal lines are alternately electrically isolated;

b. a second plurality of substantially parallel metal lines, wherein (1) the metal lines are spaced apart by spaces of width W_2, (2) each of the metal lines has a width of W_2, (3) the metal lines are alternately electrically isolated, and (4) W_1 does not equal W_2.

9. The test pattern of claim 8 wherein each of the metal lines in the first and second pluralities of substantially parallel metal lines have substantially the same length.

10. The test pattern of claim 9 wherein the length of each of the metal lines in the first and second pluralities of substantially parallel metal lines does not exceed 10 microns.

11. The test pattern of claim 10 wherein the length of each of the metal lines in the first and second pluralities of substantially parallel metal lines does not exceed 5 microns.

12. The test pattern of claim 10 wherein W_1 and W_2 do not exceed 2.5 microns.

13. The test pattern of claim 11 wherein W_1 and W_2 do not exceed 1.25 microns.

14. The test pattern of claim 8 further comprising a third plurality of substantially parallel metal lines, wherein (1) the metal lines are spaced apart by spaces of width W_3, (2) each of the metal lines has a width of W_3, (3) the metal lines are alternately electrically isolated, and (4) W_3 does not equal W_1 or W_2.

15. The test pattern of claim 8 wherein the metal lines in the first and second pluralities of substantially parallel metal lines are all of the substantially same length.

16. The test pattern of claim 8 wherein the first plurality of substantially parallel lines and the second plurality of substantially parallel lines each covers substantially the same amount of area on the semiconductor die.

17. The test pattern of claim 8 wherein the first plurality of substantially parallel lines comprises more metal lines than does the second plurality of substantially parallel lines.

18. A test pattern comprising a row of substantially parallel metal lines on a semiconductor die, the test pattern comprising:

an electrically-isolated metal line; and

a non-electrically-isolated metal line, wherein both the lines have the same width, are substantially parallel to each other and are spaced apart by their width.

19. The test pattern of claim 18 wherein the metal lines have substantially the same length.

20. The test pattern of claim 19 wherein the length of each of the metal lines does not exceed 10 microns.

21. The test pattern of claim 20 wherein the length of each of the metal lines does not exceed 5 microns.

22. The test pattern of claim 20 wherein the width of the lines does not exceed 2.5 microns.

23. The test pattern of claim 21 wherein the width of the lines does not exceed 1.25 microns.

24. A test structure for detecting defects in a semiconductor die caused by chemical mechanical polishing, the test structure comprising:

a first metal line disposed on a semiconductor die, the first metal line having a length L and width W_1 and extending in a first direction;

a second metal line disposed on a semiconductor die adjacent to the first line, the second metal line having a length L_1 and width W_1 and extending in a first direction;

a third metal line disposed on the semiconductor die adjacent to the second metal line, the third metal line having a length L_2 and width W_2 and extending in the first direction; and

a fourth metal line disposed on the semiconductor die adjacent to the third metal line, the fourth metal line having a length L_2 and width W_2 and extending in the first direction,

wherein L_1 and L_2 are not equal and the first, second, third, and fourth metal lines are alternately electrically isolated.

25. The test structure of claim 24 wherein W_1 and W_2 are not equal.

26. The test structure of claim 24 further comprising:

a fifth metal line disposed on the semiconductor die adjacent to the fourth metal line, the fourth metal line having a length L_3 and width W_3 and extending in the first direction; and

a sixth metal line disposed on the semiconductor die adjacent to the fifth metal line, the fifth metal line having a length L_3 and width W_3 and extending in the first direction,

wherein L_3 is not equal to L_1 or L_2 and the fourth, fifth, and sixth metal lines are alternately electrically isolated.

27. The test structure of claim 26 wherein W_3 is not equal to W_1 or W_2.

28. The test structure of claim 24 wherein each of L_1 and L_2 is less than 10 microns.

29. The test structure of claim 27 wherein W_1 is greater than W_2, and W_2 is greater than W_3.

30. The test structure of claim 24 wherein those metal lines that are not electrically isolated are connected to ground.

31. The test structure of claim 27 wherein each of L_1, L_2, and L_3 is less than 20 microns and each of W_1, W_2, and W_3 is less than 5 microns.

32. The test structure of claim 31 wherein each of L_1, L_2, and L_3 is less than 10 microns and each of W_1, W_2, and W_3 is less than 2 microns.

33. A row of metal test structures formed on a semiconductor die, the row of metal test structures comprising:

a. a first section, the first section comprising a first plurality of test structures, wherein the test structures of the first plurality of test structures each has the same horizontal aspect ratio; and

b. a second section, the second section comprising a second plurality of test structures, wherein the test structures of the second plurality of test structures each has the same horizontal aspect ratio but has a horizontal aspect ratio different than the horizontal aspect ratio of the first plurality of test structures.

34. A test pattern comprising a row of substantially parallel metal lines on a semiconductor die, the test pattern comprising:

a. a first plurality of substantially parallel metal lines, wherein (1) the metal lines are spaced apart by spaces of width W_1, (2) each of the metal lines has a width of W_2, (3) the metal lines are alternately electrically isolated, and (4) the sum of W_1 and W_2 is a constant K; and

b. a second plurality of substantially parallel metal lines, wherein (1) the metal lines are spaced apart by spaces of width W_3, (2) each of the metal lines has a width of W_4, (3) the metal lines are alternately electrically isolated, (4) W_1 does not equal W_3, and (5) the sum of W_3 and W_4 equals the constant K.

35. The test pattern of claim 34 wherein each of the metal lines in the first and second pluralities of substantially parallel metal lines have substantially the same length.

36. The test pattern of claim 35 wherein the length of each of the metal lines in the first and second pluralities of substantially parallel metal lines does not exceed 10 microns.

37. The test pattern of claim 36 wherein the length of each of the metal lines in the first and second pluralities of substantially parallel metal lines does not exceed 5 microns.

38. The test pattern of claim 34 wherein W_1 and W_3 do not exceed 2.5 microns.

39. The test pattern of claim 34 wherein W_1 and W_3 do not exceed 1.25 microns.

40. The test pattern of claim 34 further comprising a third plurality of substantially parallel metal lines, wherein (1) the metal lines are spaced apart by spaces of width W_5, (2) each of the metal lines has a width of W_6, (3) the metal lines are alternately electrically isolated, (4) W_5 does not equal W_1 or W_3 and (5) the sum of W_5 and W_6 equals the constant K.

41. The test pattern of claim 40 wherein the metal lines in the first, second and third pluralities of substantially parallel metal lines are all of the substantially same length.

42. The test pattern of claim 34 wherein the first plurality of substantially parallel lines and the second plurality of substantially parallel lines each covers substantially the same amount of area on the semiconductor die.

43. The test pattern of claim 34 wherein the first, second and third plurality of substantially parallel lines each comprise the same number of lines.

44. A semiconductor device, the semiconductor device comprising:

a first plurality of substantially parallel metal lines, wherein (1) the metal lines are spaced apart by spaces of width W_1, (2) each of the metal lines has a width of W_2, (3) the metal lines are alternately electrically isolated, and (4) the sum of W_1 and W_2 is a constant K; and

a second plurality of substantially parallel metal lines, wherein (1) the metal lines are spaced apart by spaces of width W_3, (2) each of the metal lines has a width of W_4, (3) the metal lines are alternately electrically isolated, (4) W_1 does not equal W_3, and (5) the sum of W_3 and W_4 equals the constant K.

45. The semiconductor device of claim 44 wherein each of the metal lines in the first and second pluralities of substantially parallel metal lines have substantially the same length.

46. The semiconductor device of claim 45 wherein the length of each of the metal lines in the first and second pluralities of substantially parallel metal lines does not exceed 10 microns.

47. The semiconductor device of claim 46 wherein the length of each of the metal lines in the first and second pluralities of substantially parallel metal lines does not exceed 5 microns.

48. The semiconductor device of claim 44 wherein W_1 and W_3 do not exceed 2.5 microns.

49. The semiconductor device of claim 44 wherein W_1 and W_3 do not exceed 1.25 microns.

50. The semiconductor device of claim 44 further comprising a third plurality of substantially parallel metal lines, wherein (1) the metal lines are spaced apart by spaces of width W_5, (2) each of the metal lines has a width of W_6, (3) the metal lines are alternately electrically isolated, (4) W_5 does not equal W_1 or W_3 and (5) the sum of W_5 and W_6 equals the constant K.

51. The semiconductor device of claim 50 wherein the metal lines in the first, second and third pluralities of substantially parallel metal lines are all of the substantially same length.

52. The semiconductor device of claim 44 wherein the first plurality of substantially parallel lines and the second plurality of substantially parallel lines each covers substantially the same amount of area on the semiconductor die.

53. The semiconductor device of claim 44 wherein the first, second and third plurality of substantially parallel lines each comprise the same number of lines.